EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	132857	(printed circuit board)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:09
S2	34	(printed circuit board) near5 optimizat$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/05 08:09
S3	1093	(circuit same routing same (optimization or optimiz$3))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/05 08:09
S4	557	(circuit same routing same (optimization or optimiz$3)) and (loop or iteration)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/05 08:10
S5	201	(circuit same routing same (optimization or optimiz$3)) and (loop or iteration) and (maximum same minimum)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/05 11:08
S6	1	"20030097243"	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/05 11:08
S7	14677	(printed near4 circuit near4 board) same array	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:45
S8	2301	(printed near4 circuit near4 board) same array and optimiz$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:45
S9	44	(printed near4 circuit near4 board) same array and optimiz$3 and (efficiency near3 (value or factor or number))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:47
S10	94	(printed near4 circuit near4 board) same array and (efficiency near3 (value or factor or number))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:48
S11	50	S10 and (not S9)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:47
S12	5753	(printed near4 circuit near4 board) same array and (value or factor or number) and (layout or placement or panel)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:49
S13	1274	(printed near4 circuit near4 board) same array and (value or factor or number) and (layout or placement or panel) and optimiz$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:49

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S14	592	(printed near4 circuit near4 board) same array and (value or factor or number) and (layout or placement or panel) and optimiz$3 and efficiency	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 15:49
S15	160	(printed near4 circuit near4 board) same array and (value or factor or number) and (layout or placement or panel) and (optimiz$3 same (layout or efficiency))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 16:04
S16	321	(circuit near4 board) same array and (value or factor or number) and (layout or placement or panel) and (optimiz$3 same (layout or efficiency))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 16:05
S17	164	S16 and (not S15)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/09 16:05
S18	191	(circuit near4 board) same (layout or placement or panel) and (optimiz$3 same (layout or efficiency)) and (efficiency same (value or factor or number))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 16:57
S19	51	circuit and (resiz$3 near3 layout)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:01
S20	150	virtuoso and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:02
S21	7	virtuoso and circuit and resiz$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:03
S22	12097	circuit and (cell same optimiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:04
S23	3659	circuit and (cell near4 optimiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:04
S24	2099	circuit and (cell near2 optimiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:04
S25	759	circuit and (cell near2 optimiz$3) and (layout or floorplan)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:04
S26	0	circuit and (cell near2 optimiz$3) and (layout or floorplan) and (outline near4 file)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:05

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S27	57	circuit and (cell near2 optimiz$3) and (layout or floorplan) and pcb	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:05
S28	0	cadence near2 layout near2 migrate	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:09
S29	0	cadence and layout near2 migrate	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:09
S30	0	cadence and layout same migrate	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:09
S31	162	circuit same layout same migrat$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/10 17:10
S32	3	circuit same layout same migrat$3 and cadence	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/12 16:31
S33	61	circuit and (cell near3 resiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:44
S34	23	circuit same (cell near3 resiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:45
S35	54	circuit same ((cell or array or block or partition) near3 resiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:45
S36	33	circuit same ((array or block or partition) near3 resiz$3)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:46
S37	0	virtuoso same circuit and ((placement or plan) near3 optimization)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:47
S38	1232	((placement or plan) near3 optimization)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:47
S39	664	((placement or plan) near3 optimization) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:48
S40	361	((placement or plan) near3 optimization) and circuit and minimum and maximum	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:48
S41	255	((placement or plan) near3 optimization) and circuit and (minimum same (size or dimension or length or width)) and maximum	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:49

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S42	213	((placement or plan) near3 optimization) and circuit and (minimum same (size or dimension or length or width)) and (maximum same (size or dimension or length or width))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 10:50
S43	142	((placement or plan) near3 optimization) and circuit and (minimum near3 (size or dimension or length or width)) and (maximum near3 (size or dimension or length or width))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:29
S44	0	(floor near2 plan$4) and ((reshap$3 or resiz$3) near3 (soft or flexible) near3 (block or cell))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:30
S45	132	(floor near2 plan$4) and ((soft or flexible) near3 (block or cell))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:31
S46	90	(floor near2 plan$4) and ((soft or flexible) near3 (block or cell)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:33
S47	0	(floor near2 plan$4) optimiz$3 and ((soft or flexible) near3 (block or cell)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:33
S48	6	((floor near2 plan$4) same optimiz$3) and ((soft or flexible) near3 (block or cell)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:47
S49	15	(floor near2 plan$4) and (gui same ((web near2 based) or internet)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:51
S50	0	(floor near2 plan$4) and (pcb same polygon) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 13:52
S51	230	(floor near2 plan$4) and polygon and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/19 14:01
S52	33	(floor near2 plan$4) and polygon and circuit and pcb	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/20 17:53
S53	602	(floor near2 plan$4) and (spac$3 and border)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/20 17:53
S54	153	(floor near2 plan$4) and (spac$3 same border)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/20 17:54
S55	8	(floor near2 plan$4) and (spac$3 same border same requirement)	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:34

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S56	1396	(floor near2 plan$4) and (rotat$3 same (cell or block or array))	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:35
S57	116	(floor near2 plan$4) and (rotat$3 near3 (cell or block or array)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:35
S58	82	(floor near2 plan$4) and (rotat$3 near2 (cell or block or array)) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:38
S59	0	(floor near2 plan$4) and (highest near2 efficien$3 same ((larg$3 or big$3) near2 (array or block or cell))) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:39
S60	0	(floor near2 plan$4) and (highest near3 efficien$3 same ((larg$3 or big$3) near3 (array or block or cell))) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:40
S61	8	(floor near2 plan$4) and (((high$3 near3 efficien$3) or (low$3 near3 cost))same ((larg$3 or big$3) near3 (array or block or cell))) and circuit	US-PGPUB; USPAT; USOCR	ADJ	ON	2006/06/21 09:54
S62	1	("5390283").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/06/21 09:54

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1 Fast printed circuit board routing
J. Dion
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Publisher: ACM Press
Full text available: pdf(930.33 KB)
Additional Information: full citation, abstract, references, citings, index terms

This paper describes the algorithms in a printed circuit board router used for fully automatic routing of high-density circuit boards. Completely automatic routing and running times of a few minutes have resulted from a new data structure for efficient representation of the routing grid, quick searches for optimal solutions, and generalizations of Lee's algorithm.

2 Use of an on-line, time-shared graphics system to design and document printed circuit boards
Leonard Marks
June 1976 **Proceedings of the 13th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(1.44 MB)
Additional Information: full citation, abstract, references, citings, index terms

A very advanced computer aided design system was recently put into operation at Martin Marietta's Orlando Division. Its purpose was to provide engineering personnel with a powerful tool for significantly lowering the cost and schedule time required to design and document complex printed circuit boards. This paper describes how the system is utilized and interfaced with related automated activities.

3 Automation of test specifications for N/C printed circuit boards
Thomas B. Yeager
June 1970 **Proceedings of the 7th workshop on Design automation**
Publisher: ACM Press
Full text available: pdf(927.89 KB)
Additional Information: full citation, abstract, references, citings, index terms

This paper presents several computer aided techniques developed by the CIMTROL Division of Cincinnati Milling Machine Co. to assist in the writing of test specifications for fault detection on printed circuit boards used in Numerical Controls. Specific capabilities of this software support are depicted, as shown in figure 1. Each of the software packages is

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1 Placement: Simultaneous block and I/O buffer floorplanning for flip-chip design

Chih-Yang Peng, Wen-Chang Chao, Yao-Wen Chang, Jyh-Herng Wang

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(253.16 KB) Additional Information: full citation, abstract, references

The flip-chip package gives the highest chip density of any packaging method to support the pad-limited ASIC design. One of the most important characteristics of flip-chip designs is that the input/output buffers could be placed anywhere inside a chip. In this paper, we first introduce the floorplanning problem for the flip-chip design and formulate it as assigning the positions of input/output buffers and first-stage/last-stage blocks so that the path length between blocks and bump balls as wel ...

2 Multi-Placement Structures for Fast and Optimized Placement in Analog Circuit Synthesis

Raoul F. Badaoui, Ranga Vemuri

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '05**

Publisher: IEEE Computer Society

Full text available: pdf(563.14 KB) Additional Information: full citation, abstract, index terms

This paper presents the novel idea of multi-placement structures, for a fast and optimized placement instantiation in analog circuit synthesis. These structures need to be generated only once for a specific circuit topology. When used in synthesis, these pre-generated structures instantiate various layout floorplans for various sizes and parameters of a circuit. Unlike procedural layout generators, they enable fast placement of circuits while keeping the quality of the placements at a high level ...

3 Combinatorial techniques for mixed-size placement

S. N. Adya, I. L. Markov

January 2005 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 10 Issue 1

Publisher: ACM Press

Full text available: pdf(1.80 MB) Additional Information: full citation, abstract, references, index terms

While recent literature on circuit layout addresses large-scale standard-cell placement, the authors typically assume that all macros are fixed. Floorplanning techniques are very good at handling macros, but do not scale to hundreds of thousands of placeable objects.